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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ANYASO, UCHENDU O	

ART UNIT	PAPER NUMBER
2675	20

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/382,677	HIROKI, MASAAKI	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. **Claims 1-29** are pending in this action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-29 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/740,944. Although the conflicting claims are not identical, they are not patentably distinct from each other because a copy of the claims (shown below) in copending Application No. 09/740,944 has the same elements as those in this instant application.

> 1. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an image signal based on a second standard clock signal; and supplying the sampled image signal to a corresponding pixel and obtaining an image.
>
> 2. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; performing frequency modulation of a second standard clock signal and obtaining a second modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an image signal based on the second modulated clock signal; and supplying the sampled image signal to a corresponding pixel and obtaining an image.

3. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an analog image signal based on a second standard clock signal, performing A/D conversion, and obtaining a digital image signal; performing D/A conversion based on the second standard clock signal after performing digital signal processing of the digital image signal, and obtaining an improved analog image signal; and supplying the improved analog image signal to a corresponding pixel and obtaining an image.

4. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; performing frequency modulation of a second standard clock signal and obtaining a second modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an analog image signal based on the second modulated clock signal, performing A/D conversion, and obtaining a digital image signal; performing
D/A conversion based on the second standard clock signal after performing digital signal processing of the digital image signal, and obtaining an improved analog image signal; and supplying the improved analog image signal to a corresponding pixel and obtaining an image.

5. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; performing frequency modulation of a second standard clock signal and obtaining a second modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an analog image signal based on the second modulated clock signal, performing A/D conversion, and obtaining a digital image signal; performing
D/A conversion based on the second modulated clock signal after performing digital signal processing of the digital image signal, and obtaining an improved analog image signal; and supplying the improved analog image signal to a corresponding pixel and obtaining an image.

6. a method of driving a semiconductor display device, comprising the steps of: performing frequency modulation of a first standard clock signal and obtaining a first modulated clock signal; performing frequency modulation of a second standard clock signal and obtaining a second modulated clock signal; selecting a gate signal line based upon the first modulated clock signal; sampling an analog image signal based on the second modulated clock signal, performing A/D conversion, and obtaining a digital image signal; performing
D/A conversion based on the second modulated clock signal after performing digital signal processing of the digital image signal, and obtaining an improved analog image signal; and supplying the improved analog image signal to a corresponding pixel and obtaining an image.

7. The method of driving a semiconductor display device according to claims 1 to 6, the modulated clock signal may also be obtained by raising or lowering the frequency of the standard clock signal at a constant period.

8. The method of driving a semiconductor display device according to claim 1 to 6, the modulated clock signal may also be obtained by shifting the frequency of the standard clock signal based on a Gaussian histogram.

9. The method of driving a semiconductor display device according to claim 1 to 6, the modulated clock signal may also be obtained by randomly shifting the frequency of the standard clock signal.

10. The method of driving a semiconductor display device according to claim 1 to claim 6, the modulated clock signal may also be obtained by sinusoidally shifting the frequency of the standard clock signal.

11. The method of driving a semiconductor display device according to claim 1 to 6, the modulated clock signal may also be obtained by shifting the frequency of the standard clock signal by using a triangular wave.

12. A semiconductor display device comprising: an active matrix circuit having a plurality of transistors arranged in a matrix shape; and a gate signal line driver circuit and a source signal line driver circuit for driving the active matrix circuit, wherein a first modulated clock signal, in which a first standard clock signal is frequency modulated, is input to the gate signal line driver circuit, and a second standard clock signal is input to the source signal line driver circuit.

13. A semiconductor display device comprising: an active matrix circuit having a plurality of transistors arranged in a matrix shape; and a gate signal line driver circuit and a source signal line driver circuit for driving the active matrix circuit; wherein a first modulated clock signal, in which a first standard clock signal is frequency modulated, is input to the gate signal line driver circuit, and a second modulated clock signal, in which a second standard clock signal is frequency modulated, is input to the source signal line driver circuit.

14. A semiconductor display device comprising a passive matrix circuit, wherein a first modulated clock signal, in which a first standard clock signal is frequency modulated, is input to a scanning electrode of the passive matrix circuit; and an image signal sampled based on a second standard clock signal is input to a signal electrode of the passive matrix circuit.

15. A semiconductor display device comprising a passive matrix circuit, wherein a first modulated clock signal, in which a first standard clock signal is frequency modulated, is input to a scanning electrode of the passive matrix circuit; and an image signal sampled based on a second modulated clock signal,in which a second standard clock signal is frequency modulated, is input to a signal electrode of the passive matrix circuit.

16. The semiconductor display device according to claims 12 to 15, the modulated clock signal may also be obtained by raising or lowering the frequency of the standard clock signal at a constant period.

17. The semiconductor display device according to claim 12 to 15, the modulated clock signal may also be obtained by shifting the frequency of the standard clock signal based on a Gaussian histogram.

18. The semiconductor display device according to claim 12 to 15, the modulated clock signal may also be obtained by randomly shifting the frequency of the standard clock signal.

19. The semiconductor display device according to claim 12 to 15, the modulated clock signal may also be obtained by sinusoidally shifting the frequency of the standard clock signal.

20. semiconductor display device according to claim 12 to 15, the modulated clock signal may also be obtained by shifting the frequency of the standard clock signal by using a triangular wave.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 5-7** and **17-19** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to **claims 5** and **17**, applicant claims how a modulated clock signal may be obtained by randomly shifting the frequency of the standard clock signal. However, the specification does not describe this concept to enable one skilled in the art to make and/or use this concept of randomly shifting the frequency of the standard clock signal.

With respect to **claim 6, 7, 18** and **19**, applicant claims a modulated clock signal that may be obtained by shifting the frequency of the standard clock signal in the form of a triangular wave and sine wave. However, the specification does not describe this concept to enable one skilled in the art to make and/or use this concept of obtaining a modulated clock signal by shifting the frequency of the standard clock signal in the form of a triangular wave and sine wave.

Applicant is advised to clarify these concepts.

Claim Rejections - 35 USC ' 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. **Claims 1, 5, 12, 13 and 17** are rejected under 35 U.S.C. 102(e) as being anticipated by *Bassetti et al* (U.S. Patent 6,046,735).

Regarding **Claims 1, 12, 13**, Bassetti teaches a video clock that has a constant frequency wherein a modulated video clock means supplies a frequency-modulated video clock to the flat-panel converter such that the flat-panel converter transfers pixels out the panel-interface output to the flat-panel display at a modulated rate proportional to a current frequency of the frequency-modulated video clock (column 6, lines 19-24).

Furthermore, Bassetti teaches applying a modulated clock signal to a source signal line-side driving circuit of a display device by teaching how a clock modulator 82' generates modulated video clock VCLK_SS by slowly decrementing the frequency while pixels are being written to a first half of a horizontal line, but then slowly incrementing the frequency while pixels are being written to a second half of the horizontal line (column 14, lines 62 through column 15, line 4, figure 13 at 82'). Also, Bassetti further teaches that the modulated video clock VCLK_SS is input to the entire CRT path and the LCD path, including CRT buffer 52, attribute controller 54, RAM look-up table 56, and LCD controller 62 (column 15, lines 5-11).

Furthermore, Bassetti discloses how his device would be used in an active matrix type device by disclosing the use of his within a TFT-type display (column 1, lines 57-59).

Furthermore, Bassetti teaches how to supply the sampled image to a corresponding pixel to obtain an image (column 6, lines 35-37).

Regarding **Claims 5 and 17**, in further discussion of claims 1 and 12, Bassetti discloses how a modulated clock signal may be obtained by randomly shifting the frequency of the modulated clock (column 5, lines 30-36).

Claim Rejections - 35 USC ' 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 2, 3** and **8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bassetti et al* (U.S. Patent 6,046,735) in view of *Taguchi* (U.S. Patent 6,115,020).

Regarding **Claim 2** and **3**, Bassetti teaches a video clock that has a constant frequency wherein a modulated video clock means supplies a frequency-modulated video clock to the flat-panel converter such that the flat-panel converter transfers pixels out the panel-interface output to the flat-panel display at a modulated rate proportional to a current frequency of the frequency-modulated video clock (column 6, lines 19-24).

Furthermore, Bassetti teaches how to obtain a modulated clock signal by teaching how a clock modulator 82' generates modulated video clock VCLK_SS by slowly decrementing the frequency while pixels are being written to a first half of a horizontal line, but then slowly incrementing the frequency while pixels are being written to a second half of the horizontal line (column 14, lines 62 through column 15, line 4, figure 13 at 82'). Also, Bassetti further teaches that the modulated video clock VCLK_SS is input to the entire CRT path and the LCD path, including CRT buffer 52, attribute controller 54, RAM look-up table 56, and LCD controller 62 (column 15, lines 5-11)..

Furthermore, Bassetti discloses how his device would be used in an active matrix type device by disclosing the use of his within a TFT-type display (column 1, lines 57-59).

Furthermore, Bassetti teaches how to supply the sampled image to a corresponding pixel to obtain an image (column 6, lines 35-37).

Also, Bassetti teaches a digital-to-analog converter (DAC) that is coupled to receive pixels from the pixel output of the pixel-transfer path (column 6, lines 28-30; column 15, lines 46-67, figure 15 at 114).

However, Bassetti does not teach an analog-to-digital converter (A/D) that samples an analog signal. On the other hand, Taguchi teaches an invention that pertains to a display method capable of enlarging an image in the vertical direction at an arbitrary enlargement ration wherein an A/D converter 621 converts an analog image signal onto n-bit digital signals (column 3, lines 51-55; column 25, lines 39-52, figure 45 at 621).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Bassetti and Taguchi inventions because while Bassetti teaches how to frequency modulate a

video clock signal, Taguchi teaches how to achieve A/D conversion in such a device. The motivation for combining these inventions would have been to efficiently enlarge an image in a display device without causing adverse effects such as flicker noise appearing on the image (column 3, lines 41-55).

Regarding **Claims 8-11**, in further discussion of claim 2, Bassetti discloses how his device would be used in an active matrix type device by disclosing the use of his within a TFT-type display (column 1, lines 57-59). It is well known in the art how such a display would be an active matrix type display device, passive matrix type display device, liquid crystal type display device or an electroluminescence display.

10. **Claim 4** and **16** is rejected under 35 U.S.C. 103(a) as being unpatentable over *Bassetti et al* (U.S. Patent 6,046,735) in view of *Oakley* (U.S. Patent 6,281,873).

Regarding **Claims 4** and **16**, in further discussion of claim 1 and 12, Bassetti does not teach a method wherein the modulated clock is obtained by shifting a frequency of the reference clock signal on the basis of a gaussian histogram. On the other hand, Oakley teaches a video processing technique related to a vertical scaling process and apparatus wherein each frame of the image consists of a collection of horizontal scan lines which are intensity modulated to form an image by decreasing the frequency of the incoming sampling clock or increasing the frequency of the encoder pixel clock (*see* column 3, lines 1-25; *see also* column 1, lines 5-7). *Oakley* goes on to teach that by changing a gaussian filter coefficients of the kernel, the output can be time shifted by fractions of the clock period (column 4, lines 6-18).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Bassetti and Oakley's inventions because while the combination of Bassetti teaches how to frequency modulate a video clock signal, Oakley teaches changing a gaussian filter coefficients of the kernel so that the output can be time shifted by fractions of the clock period (column 4, lines 6-18). The motivation for combining these inventions would have been to scale down or shrink video frames in a horizontal or vertical direction (*see* column 1, lines 64-67).

11. **Claims 6, 7, 18** and **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bassetti et al* (U.S. Patent 6,046,735) in view of *Guttner* (U.S. Patent 4,713,688).

Regarding **Claims 6, 7, 18** and **19**, in further discussion of claim 1 and 12, Bassetti does not teach a display device wherein the modulated clock signal is obtained by shifting a frequency of the reference clock signal in the form of a sine wave or triangular wave. On the other hand, *Guttner* teaches offset rasters that facilitate the offset demodulation process (column 11, lines 6-20; *see also* column 8, lines 45-58, figure 10) wherein the picture signal spectrum is periodic in the direction of the horizontal spatial frequencies due to the horizontal sampling in the spatial domain (column 5, lines 51-65, figure 3). Figure 3 shows the clock signal in the form of a sine wave.

Thus, it would have been obvious to a person of ordinary skill in the art to combine Bassetti and *Guttner* inventions because while Bassetti teaches how to frequency modulate a video clock signal, *Guttner* teaches how the shifting of the clock signal would be represented in the form of a periodic sine wave or triangular wave. The motivation for combining these

inventions would have been to transmit an image signal with significantly improved horizontal resolution (*see generally* column 1, lines 11-18).

12. **Claims 14, 15 and 20-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Bassetti et al* (U.S. Patent 6,046,735) in view of *Martin et al* (U.S. Patent 5,703,621).

Regarding **Claims 14** and **15**, Bassetti teaches a video clock that has a constant frequency wherein a modulated video clock means supplies a frequency-modulated video clock to the flat-panel converter such that the flat-panel converter transfers pixels out the panel-interface output to the flat-panel display at a modulated rate proportional to a current frequency of the frequency-modulated video clock (column 6, lines 19-24).

However, Bassetti does not teach the display device having passive matrix circuit. On the other hand, Martin teaches techniques for presenting all images types such as video images (column 1, lines 45-49) wherein the display includes a monochrome display (claim 9, column 20, lines 54-56) wherein an image signal would be inputted to a signal electrode of the passive matrix circuit (column 14, lines 1-8, figure 4 at 122, 130, 132, 134). Martin also teaches that his invention is capable of performing any necessary scaling, cropping and segmentation of the input image (column 14, lines 9-19, figure 5 at 140 & 142).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Bassetti and Martin teachings in designing a display device wherein Bassetti teaches how to frequency modulate a video clock signal and Martin teaches a monochrome display device with scaling, cropping and segmentation capabilities. The motivation for combining these inventions

would have been to present high quality images in the display device (column 4, lines 66-67 *through* column 5, line 1).

Regarding **Claims 20** and **21**, in further discussion of claim 12, *Martin* teaches that his display device could be an LCD, an electroluminescent display or any other type of display (column 18, lines 62-67).

Regarding **Claims 22-29**, in further discussion of claim 12, it is well known in the art that devices such as a mobile telephone, projector, video camera, mobile computer, head mounted display, personal computer, recorder and a digital camera all comprise a display device. Thus, it would have been obvious to a person skilled in the art to utilize such a display device as described in *Bassetti and Martin* in these equipment.

Response to Arguments

13. Applicant's arguments filed July 2, 2003 have been fully considered but they are not persuasive.

Applicant argues the rejections based on 35 U.S.C. 112, first paragraph, for lack of enablement. Specifically, applicant argues that the concept of randomly shifting a frequency of a reference clock signal, or shifting a frequency of a reference clock signal in the form of either a sine wave or a triangular wave are taught in the specification on page 7, paragraph 4-6, and page 15. Examiner reviewed page 7, paragraph 4-6, and concludes that these aspects of the specification are a mere regurgitation of the claims, and thus, does not describe these concept to

enable one skilled in the art to make and/or use this concept of obtaining a modulated clock signal by shifting the frequency of the standard clock signal in the form of a triangular wave and sine wave.

Also, page 15 was reviewed with respect to the concept of randomly shifting a reference clock. However, the specification clearly states that the reference clock operates at a constant frequency, and the modulated clock signal is a clock signal, which shifts in frequency at a certain constant period. This concept as espoused in the specification seems to be teaching away from the concept randomly shifting the reference clock because this same reference clock operates at a constant frequency. As such, the lack of enablement rejection is maintained for claims 5-7 and 17-19.

Furthermore, with respect to claims 1 and 12, applicant argues the rejection based on 35 U.S.C. 102(e) as being anticipated by *Bassetti et al* (U.S. Patent 6,046,735). Specifically, applicant contends that Bassetti does not teach the concept of applying or inputting a modulated clock signal to a source signal line-side driver circuit. Examiner disagrees with this assertion because Bassetti teaches how a clock modulator 82' generates modulated video clock VCLK_SS by slowly decrementing the frequency while pixels are being written to a first half of a horizontal line, but then slowly incrementing the frequency while pixels are being written to a second half of the horizontal line (column 14, lines 62 through column 15, line 4, figure 13 at 82'). Also, Bassetti further teaches that the modulated video clock VCLK_SS is input to the entire CRT path and the LCD path, including CRT buffer 52, attribute controller 54, RAM look-up table 56, and LCD controller 62 (column 15, lines 5-11).

With respect to claims 2, 3, and 8-11, applicant argues that Bassetti and Taguchi do not teach performing sampling and A/D conversion on an analog image signal on the basis of a modulated clock signal, and performing D/A conversion on a digital image signal on the basis of a modulated clock signal. Examiner disagrees. This is because Bassetti teaches how to obtain a modulated clock signal by teaching how a clock modulator 82' generates modulated video clock VCLK_SS by slowly decrementing the frequency while pixels are being written to a first half of a horizontal line, but then slowly incrementing the frequency while pixels are being written to a second half of the horizontal line (column 14, lines 62 through column 15, line 4, figure 13 at 82'). Also, Bassetti further teaches that the modulated video clock VCLK_SS is input to the entire CRT path and the LCD path, including CRT buffer 52, attribute controller 54, RAM look-up table 56, and LCD controller 62 (column 15, lines 5-11)..

Furthermore, Bassetti teaches how to supply the sampled image to a corresponding pixel to obtain an image (column 6, lines 35-37) wherein a digital-to-analog converter (DAC) is coupled to receive pixels from the pixel output of the pixel-transfer path (column 6, lines 28-30; column 15, lines 46-67, figure 15 at 114). Although Bassetti does not teach an analog-to-digital converter (A/D) that samples an analog signal Taguchi teaches an invention that pertains to a display method capable of enlarging an image in the vertical direction at an arbitrary enlargement ration wherein an A/D converter 621 converts an analog image signal onto n-bit digital signals (column 3, lines 51-55; column 25, lines 39-52, figure 45 at 621).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Bassetti and Taguchi inventions because while Bassetti teaches how to frequency modulate a video clock signal, Taguchi teaches how to achieve A/D conversion in such a device. The

motivation for combining these inventions would have been to efficiently enlarge an image in a display device without causing adverse effects such as flicker noise appearing on the image (column 3, lines 41-55).

As such, applicant's assertion that contends that Bassetti and Taguchi do not teach performing sampling and A/D conversion on an analog image signal on the basis of a modulated clock signal, and performing D/A conversion on a digital image signal on the basis of a modulated clock signal is not persuasive.

With respect to claims 14 and 15, applicant argues that nothing in Bassetti or Martin teaches how an image signal should be input to a signal electrode of a passive matrix circuit. However, Martin teaches techniques for presenting all images types such as video images (column 1, lines 45-49) such that the display includes a monochrome display (claim 9, column 20, lines 54-56) wherein an image signal would be inputted to a signal electrode of the passive matrix circuit (column 14, lines 1-8, figure 4 at 122, 130, 132, 134).

Hence, applicant's amendments and arguments are not persuasive.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Uchendu O. Anyaso** whose telephone number is **(703) 306-5934.** If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Steve Saras**, can be reached at **(703) 305-9720.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

May 25, 2004

CHANH NGUYEN
PRIMARY EXAMINER